Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 30536

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024

Fifth Semester

Electronics and Communication Engineering

EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Differentiate between the instructions MOVE R4, R5 and LOAD R4, (R5) with respect to the addressing mode.

2. Express the throughput of non-pipelined architectures as a function of clock cycles per instruction and clock rate of the processor.

3. What is the least negative number that can be represented using the 8-bit 2's – complement number system?

4. Outline the significance of Booth's algorithm in arithmetic design of computers.

5. Mention the purpose of multiplexers in logic design of processors.

6. Interpret the different types of hazards of pipelined architectures.

7. Compare and contrast cache and virtual memories in terms of cost, speed and size.

8. List the criteria that decides whether to use parallel or serial bus architectures for Input/Output interfacing.

9. Differentiate coarse – grained and fine-grained multi-threading techniques.

10. List the different types of interconnection networks used in multiprocessor architecture.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Suppose that a processor needs to be interfaced with 1 GigaBytes of memory. Determine the minimum number of address lines required by this processor architecture. (6)

(ii) Discuss zero-address, one-address and two-address instructions with examples. (7)

Or

(b) Define addressing mode. Classify various addressing modes and illustrate them with suitable instruction mnemonics as examples. (13)

12. (a) (i) Summarize the steps involved in multiplication of two 'n' bit numbers giving suitable example. (8)

(ii) Explain the terms mantissa and exponent. (5)

Or

(b) Describe the organization of carry-save-adder for implementation of fast multipliers. Summarize the steps involved in multiplying the numbers : (–13) and (7). (13)

13. (a) Summarize the datapath of a five-stage pipelined processor architecture with a neat data flow diagram. (13)

Or

(b) (i) Explain Superscalar processor architecture. (6)

(ii) Explain the possibility of pipeline hazards that could happen due to data dependently with suitable sequence of instruction mnemonics. (7)

14. (a) Distinguish between static and dynamic memories with respect to their internal organization and read/write mechanisms. (13)

Or

(b) Explain the following bus standards PCI, USB and SATA. (13)

15. (a) (i) Distinguish between Uniform Memory Access and Non-Uniform Memory Access architectures for multiprocessors. (6)

(ii) Compare and contrast GPU with traditional CPU. (7)

Or

(b) (i) Compare the ring type networking of multiprocessors with that of bus type. (6)

(ii) Explain multicore architecture giving suitable examples for the state-of-the-art architectures. (7)

PART C — (1 × 15 = 15 marks)

16. (a) Design a computer system in which a 16-bit processor is interfaced with 128 KB of ROM and 512 KB of RAM. Explain the design with a neat sketch of interconnection diagram and decoding logic. Assume that the processor has 24 address lines with low-order address lines multiplexed with data bus.

Or

(b) Consider the following instruction sequence :

2000 : Add R3, R2, #100

2004 : Subtract R5, R4, #1

2008 : Or R6, R4, Ox55

2012 : Add R7, R2, R4

Initially the registers R2 and R4 contain 1000 and 100, respectively. These instructions are executed in a computer that has a five-stage pipeline. The first instruction is fetched in clock cycle 1 and the remaining instructions are fetched in successive cycles.

Draw a timing diagram that represents the flow of the instructions through the pipeline. Describe the operation being performed by each pipeline stage during clock cycles 1 through 8.